

Electronic Information Disclosure Statement

TESTING LOGIC AND EMBEDDED MEMORY IN PARALLEL

#4
JC474 U.S. PTO
10/065503
10/25/02

Application:

Confirmation:

Applicant(s): William Corbin

Docket Number: BUR920010217

Group Art





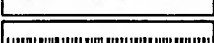
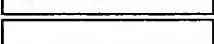

Unit:

Examiner:

search string: (5987635 or 3961251 or 4481627 or 5996097 or 5954830 or 6044481 or 6324107 or 6111800 or 5903576 or 5892721 or 5663965 or 5436910 or 6125460 or 5535164).pn.

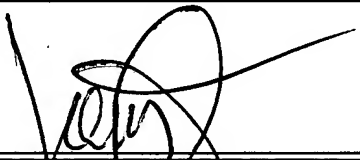
US Patent Documents

Note: Applicant is not required to submit a paper copy of cited US Patent Documents

init	Citation No.	Patent Number	Date	Bar Code	Patentee	Class	Subclass
P01	5987635	1999-11-16		Kishi et al.			
P02	3961251	1976-06-01		Hurley et al.			
P03	4481627	1984-11-06		Beauchesne et al.			
P04	5996097	1999-11-30		Evans et al.			
P05	5954830	1999-09-21		Ternullo			
P06	6044481	2000-03-28		Kornachuk et al.			
P07	6324107	2001-11-27		Allan et al.			

P08	6111800	2000-08-29		Allan et al.
P09	5903576	1999-05-11		Yoshiba
P10	5892721	1999-04-06		Kim
P11	5663965	1997-09-02		Seymour
P12	5436910	1995-07-25		Takeshima et al.
P13	6125460	2000-09-26		Sim
P14	5535164	1996-07-09		Adams et al.

Signature

Examiner Name	Date
	6/5/2004